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(54) **Power MOSFET semiconductor device and method of manufacturing the same**

(57)   A semiconductor device includes a semiconductor substrate (11) of a first conductivity type, on which a semiconductor layer (12) having a trench (15) extending in the depth direction toward the semiconductor substrate (11) is formed. A first region (19) of the first conductivity type is formed in the depth direction along one side of the trench (15) in the semiconductor layer (12) and contacts the semiconductor substrate (11). A second region (25) of the first conductivity type is formed in a surface area of the semiconductor layer (12) and close to the trench (15) and contacts the first region (19). A third region (26) of the second conductivity type is formed in the surface area of the semiconductor layer (12). A fourth region (27) of the first conductivity type is formed in a surface area of the third region (26). A gate insulation film and a gate electrode (29) are provided on the surface of the third region (26) between the second region (25) and the fourth region (27).
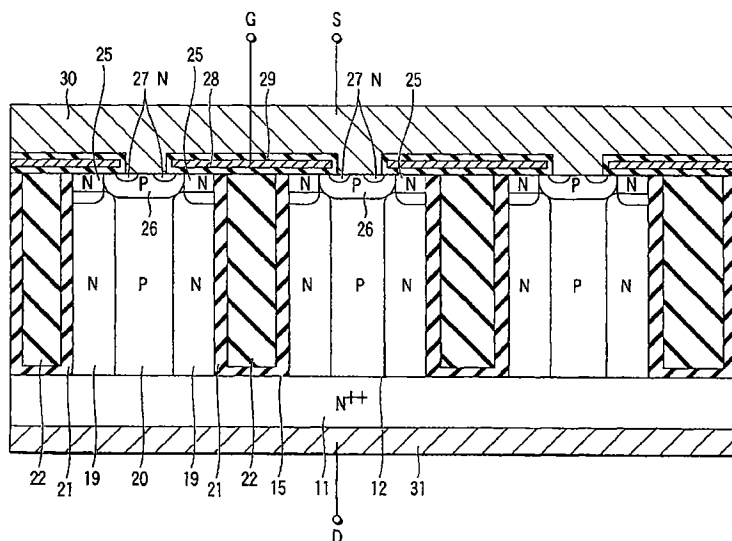
FIG. 1

Description

[0001] The present invention relates to a power MOS-FET semiconductor device used for control of high power and a method of manufacturing the semiconductor device.

[0002] A deep trench MOSFET (referred to as DT-MOS hereinafter) has recently been proposed as a power-switching device using a MOSFET.

[0003] A semiconductor device according to a first aspect of the present invention comprises a semiconductor substrate of a first conductivity type, a semiconductor layer provided on the semiconductor substrate, a trench extending in a depth direction toward the semiconductor substrate from a surface of the semiconductor layer, a first region of the first conductivity type formed in the depth direction on and along a side of the trench in the semiconductor layer, a bottom of the first region contacting the semiconductor substrate, a second region of the first conductivity type formed in a surface area of the semiconductor layer and close to the side of the trench, the second region contacting the first region, a third region of the second conductivity type formed in the surface area of the semiconductor layer, a fourth region of the first conductivity type formed in a surface area of the third region, and a gate electrode provided on a surface of the third region between the second region and the fourth region, a gate insulation film being interposed between the gate electrode and the second region.

[0004] A method of manufacturing a semiconductor device according to a second aspect of the present invention, comprises forming a semiconductor layer on a semiconductor substrate of a first conductivity type, forming a trench having a first opening in the semiconductor layer, the trench extending in a depth direction toward the semiconductor substrate, ion-implanting first and second impurities into an inner wall of the trench through the first opening, diffusing the first impurities to form a first region of the first conductivity in the depth direction on and along a side of the trench in the semiconductor layer, a bottom of the first region contacting the semiconductor substrate, diffusing the second impurities to form a second region of a second conductivity type in the depth direction along the first region in the semiconductor layer, the second region contacting one side of the first region, which is opposite to another side contacting the trench, burying a filling layer into the trench, forming a third region of the first conductivity type in a surface area of the semiconductor layer and close to the side of the trench, the third region contacting the first region, forming a fourth region of the second conductivity type in the surface area of the semiconductor layer, the fourth region having impurity concentration which is higher than that of the second region, and forming a fifth region of the first conductivity type in a surface area of the fourth region.

[0005] This summary of the invention does not necessarily describe all necessary features so that the in-

vention may also be a sub-combination of these described features.

[0006] The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic cross-sectional view of a semiconductor device according to a first embodiment of the present invention.

FIG. 2 is a cross-sectional view showing a manufacturing step of the semiconductor device of FIG. 1.

FIG. 3 is a cross-sectional view showing a manufacturing step subsequent to the step of FIG. 2.

FIG. 4 is a cross-sectional view showing a manufacturing step subsequent to the step of FIG. 3.

FIG. 5 is a cross-sectional view showing a manufacturing step subsequent to the step of FIG. 4.

FIG. 6 is a cross-sectional view showing a manufacturing step subsequent to the step of FIG. 5.

FIG. 7 is a cross-sectional view showing a manufacturing step subsequent to the step of FIG. 6.

FIG. 8 is a cross-sectional view showing a manufacturing step subsequent to the step of FIG. 7.

FIG. 9 is a cross-sectional view showing a manufacturing step subsequent to the step of FIG. 8.

FIG. 10 is a cross-sectional view showing a manufacturing step subsequent to the step of FIG. 9.

FIG. 11 is a cross-sectional view of the semiconductor device shown in FIG. 1, which shows a contour map of the distribution of concentrations of an N-type pillar layer.

FIG. 12 is a graph of the distribution of concentrations in the cross-sectional view taken along line XII-XII of FIG. 11.

FIG. 13 is a graph of the distribution of concentrations in the cross-sectional view taken along line XIII-XIII of FIG. 11.

FIGS. 14A and 14B are cross-sectional views of the semiconductor device according to first and second modification of the first embodiment of the present invention.

FIG. 15 is a schematic cross-sectional view of a semiconductor device according to a second embodiment of the present invention.

FIG. 16 is a schematic cross-sectional view showing a manufacturing step of the semiconductor device according to the second embodiment of the present invention, which is subsequent to the step shown in FIG. 9.

FIG. 17 is a contour map of the distribution of concentrations of an N-type pillar layer in the semiconductor device shown in FIG. 15.

FIG. 18 is a map of the distribution of concentrations taken along line XVIII-XVIII of FIG. 17.

FIG. 19 is a map of the distribution of concentrations taken along line XIX-XIX of FIG. 17.

FIG. 20 is a schematic cross-sectional view of a

semiconductor device according to a third embodiment of the present invention.

FIG. 21 is a schematic cross-sectional view showing a manufacturing step of the semiconductor device according to the third embodiment of the present invention, which is subsequent to the step shown in FIG. 9.

FIG. 22 is a schematic cross-sectional view of a semiconductor device with a DTMOS having an ideal structure.

FIG. 23 is a cross-sectional view explaining a problem of the manufacturing step of a semiconductor device of FIG. 22.

FIG. 24 is cross-sectional view showing a manufacturing step subsequent to the step of FIG. 23.

FIG. 25 is a contour map of the distribution of concentrations of an N-type pillar layer of a semiconductor device of FIG. 24.

FIG. 26 is a cross-sectional view explaining a problem of the manufacturing step of a semiconductor device of FIG. 22.

FIG. 27 is a cross-sectional view explaining a problem of the manufacturing step of a semiconductor device of FIG. 22.

FIG. 28 is cross-sectional view showing a manufacturing step subsequent to the step of FIG. 27.

FIG. 22 is a schematic cross-sectional view of a DTMOS having an ideal structure. The DTMOS has a socalled super junction structure in which N- and P-type pillar layers 119 and 120 serving as a current path are formed in the depth (vertical) direction between trenches 115. As shown in FIG. 22, a low-concentration N$^-$-type semiconductor layer 112 is provided on a high-concentration N$^+$-type semiconductor substrate (silicon substrate) 111. A deep trench 115 is formed in the semiconductor layer 112. An N-type pillar layer 119 is formed on either side of the trench 115 in the semiconductor layer 112. The top of the N-type pillar layer 119 reaches the surface of the semiconductor layer 112. A P-type pillar layer 120 is formed adjacent to the N-type pillar layer 119. A buried layer 122 is formed as an element isolating insulation film in the trench 115 with an oxide film 121 interposed therebetween.

[0007]   A high-concentration P$^+$-type base layer 126 is formed in the surface area of the semiconductor layer 112, and a high-concentration N$^+$-type source layer 127 is formed in the surface area of the base layer 126. A gate electrode 128 is formed on the semiconductor layer 112 with a gate insulation film interposed therebetween. The gate electrode 128 is covered with an interlayer insulation film 129. A source electrode 130 is formed on the interlayer insulation film 129, and a drain electrode 131 is formed on the undersurface of the substrate 111.

[0008]   The super junction structure allows the devices to increase in withstand voltage and to decrease in on-resistance.

[0009]   The inventors of the present invention studied a manufacturing process of the DTMOS as shown in FIG. 22 in the process of development of the present invention and obtained the following findings.

[0010]   First, a method of manufacturing a DTMOS having a structure as described above will be described in brief with reference to FIG. 22. A semiconductor layer 112 is formed on a semiconductor substrate 111 by epitaxial growth. A mask layer is formed on the semiconductor layer 112 and then patterned. Using the patterned mask layer as a mask, a deep trench 115 is formed in the semiconductor layer 112 by anisotropic etching. N-type and P-type impurities are implanted into the inner walls of the trench 115 and diffused thermally, thereby forming an N-type pillar layer 119 and a P-type pillar layer 120 along the trench 115. After that, a buried layer 122 is formed in the trench 115 with an oxide layer 121 interposed therebetween.

[0011]   A base layer 126 is selectively formed in a surface area of the semiconductor layer 112 and a source layer 127 is selectively formed in the base layer 126. Then, a gate electrode 128 is formed on the semiconductor layer 112 with a gate insulation film interposed therebetween and covered with an interlayer insulation film 129. A source electrode 130 is formed on the interlayer insulation film 129 and a drain electrode 131 is formed on the undersurface of the substrate 111.

[0012]   The DTMOS formed through the above process does not have any ideal structure as shown in FIG. 22 and thus causes the following problems.

[0013]   When a deep trench 115 is formed in the semiconductor layer 112 by anisotropic etching using the mask layer 113 as shown in FIG. 23, the semiconductor layer 112 is etched more widely than the opening of the mask layer 113, and the mask layer 113 overhangs the trench 115. Such a structure is called an overhang. If a trench 115 having a depth of 60 μm by anisotropic etching having a large directional selective etching ratio of, e.g., 200, the inner walls of the trench 115 each retreats by 0.3 μm to form projected portions 113a of the mask layer 113. When ions are implanted into the inner wall of the trench 115 at a low angle leaving the projected portions 113a as they are, the projected portions 113a become a barrier against ion implantation.

[0014]   Though the ion-implanted impurities are thermally diffused, no N-type pillar layer 119 is formed on the side of the trench 115 in the upper region of the semiconductor layer 112, as shown in FIGS. 24 and 25. In other words, the N-type pillar layer 119 does not reach the surface of the semiconductor layer 112. When the length of a projected portion 113a is 0.3 μm and the angle of ion implantation is 7°, the length X (corresponding to the distance from the surface of the semiconductor layer 112 to the end of the N-type pillar layer 119) of a region into which no impurities are ion-implanted is 2.4 μm. When the angle of ion implantation is 5°, distance X is 3.4 μm.

[0015]   When the N-type pillar layer 119 does not

reach the surface of the semiconductor layer 112, a current path of a MOSFET having a vertical PN junction is cut off; therefore, the MOSFET does not operate normally even though a channel is formed in an inverted region. In order to resolve this problem, the N-type pillar layer 119 needs to be formed up to the surface of the semiconductor layer 112.

[0016] As a first method, after the trench 115 is formed using the mask layer 113, the opening of the mask layer 113 can be broadened more than that of the trench 115 by isotropic etching and then ion-implantation can be performed. Taking into consideration variations in the amount of overhang and the amount of isotropic etching within a wafer, however, it is difficult to broaden the opening of the mask layer 113 by a desired amount in each of trenches 115 within the wafer. If the opening of the mask layer 113 is broadened too much as shown in FIG. 26, the surface of the semiconductor layer 112 is exposed to cause an exposed region 112a to appear. Since impurities are ion-implanted into the inner wall of the trench 115 at a low angle, a dose of impurities is high. When ions are implanted into the exposed region 112a, the concentration of the region 112a becomes very high, which exerts an influence upon the characteristics of the MOSFET formed on a semiconductor layer 112 and the shape of a diffusion layer. If the concentration of the exposed region 112a is high especially when a super junction is formed by ion-implanting N- and P-type impurities into the inner wall of the trench 115 and simultaneously diffusing them, the reverse bias withstand voltage of the elements will be lowered.

[0017] As a second method, the upper region of the semiconductor layer 112 where the N-type pillar layer 119 is not formed can be removed. In other words, impurities are ion-implanted and diffused into the trench 115 leaving the projected portions 113a of the mask layer 113 as they are, and then the mask layer 113 is removed. As shown in FIG. 27, a buried layer 122 is formed in the trench 115 with an oxide film 121 interposed therebetween. After that, as shown in FIG. 28, the semiconductor layer 112, oxide film 121, and buried layer 122 are removed by, e.g., polishing until the upper region of the semiconductor layer 112 where the N-type pillar layer 119 is not formed disappears. The surfaces of the layer 112, film 121 and layer 122 are flattened. In this case, however, the semiconductor layer 112 has to be epitaxially grown thickly in advance by the amount of flattening and elimination, the manufacturing costs will be increased.

[0018] It is difficult to form the N-type pillar layer 119 up to the surface of the semiconductor layer 112 in the foregoing process. Consequently, it is difficult to resolve the problem that a source-to-drain current path is cut off.

[0019] Embodiments of the present invention developed on the basis of the foregoing findings will now be described with reference to the accompanying drawings. The components having substantially the same function and structure are denoted by the same reference numerals and their descriptions are repeated only when the need arises.

[0020] The embodiments of the present invention relates to a power MOSFET and more specifically to a DT-MOS having a vertical NPN structure. In this DTMOS, an N-type pillar layer serving as a current path and a P-type pillar layer for maintaining a reverse withstand voltage between drain and source regions are formed in the depth direction between trenches formed in a semiconductor layer.

[First Embodiment]

[0021] FIG. 1 is a schematic cross-sectional view showing a semiconductor device according to a first embodiment of the present invention as a DTMOS having a vertical NPN structure. The first embodiment is directed to an N-channel DTMOS. However, the present invention can be applied to a P-channel DTMOS by varying impurities appropriately.

[0022] As depicted in FIG. 1, a low-concentration N⁻-type semiconductor layer 12 is provided on a high-concentration N⁺⁺-type semiconductor substrate (silicon substrate) 11. The semiconductor layer 12 can be of a low-concentration P⁻-type. A deep trench 15 extends in the depth direction toward the substrate 11 through the semiconductor layer 12. The trench 15 reaches the semiconductor substrate 11. A buried layer (filling layer) 22, which is composed of one of polysilicon, amorphous silicon, and a dielectric, is formed in the trench 15 through an oxide film 21 provided on the surface of the trench 15. The trench 15 is filled with the buried layer 22. The buried layer 22 serves as an element isolating insulation film. The oxide film 21 isolates the semiconductor layer 12 and the buried layer 22 from each other.

[0023] A first N-type pillar layer 19 is formed along and on either side of the trench 15 in the depth direction. The top of the pillar layer 19 is located away from the surface of the semiconductor layer 12 and the bottom thereof contacts the semiconductor substrate 11. A P-type pillar layer 20 contacts one side of the first N-type pillar layer 19, which is opposite to the other side contacting the trench 15. The pillar layer 20 is formed in the depth direction along the pillar layer 19. Thus, a super junction structure is obtained.

[0024] A second N-type pillar layer 25 is provided on either side of the trench 15 in the surface area of the semiconductor layer 12. The top of the pillar layer 25 reaches the surface of the semiconductor layer 12 and the bottom portion thereof overlaps the top portion of the first N-type pillar layer 19. Consequently, the first and second N-type pillar layers 19 and 25 are electrically connected to each other. These pillar layers 19 and 25 serve as a source-to-drain current path.

[0025] A high-concentration P⁺-type base layer 26 is provided between adjacent second N-type pillar layers 25 in the surface area of the semiconductor layer 12. Ends of the base layer 26 may contact the second N-

type pillar layer 25 and a corner of the layer 26 may contact the first N-type pillar 19. A high-concentration N+-type source layer 27 is formed in the surface area of the P+-type base layer 26. One end of the source layer 27 is located at a given distance from that of the base layer 26. A gate electrode 28 is formed on the semiconductor layer 12 with a gate insulation film interposed therebetween. The gate electrode 28 is covered with an interlayer insulation film 29. The gate electrode 28 and interlayer insulation film 29 are formed above at least the trench 15 and their ends extend to a region between the base layer 26 and source layer 27. This region serves as a channel. A source electrode 30 is formed on the interlayer insulation film 29 and a drain electrode 31 is formed on the undersurface of the substrate 11.

[0026] FIGS. 2 to 11 are schematic cross-sectional views each showing a manufacturing step of the semiconductor device described above. A method of manufacturing the semiconductor device will be described below.

[0027] First, as shown in FIG. 2, a semiconductor layer 12 is formed on a semiconductor substrate 11 by epitaxial growth. A mask layer 13 is formed on the surface of the semiconductor layer 12. The mask layer 13 is a two-layered film including a thermal oxide film and a CVD (chemical vapor deposition) film.

[0028] Then, as shown in FIG. 3, the mask layer 13 is patterned by lithography and etching to form an opening 14 through which part of the surface of the semiconductor layer 12 is exposed to the mask layer 13. Anisotropic etching is performed using the mask layer 13 with the opening 14 as a mask to form a trench 15 that reaches into the substrate 11 through the semiconductor layer 12.

[0029] It is desirable that the etching for forming the trench 15 be performed using an apparatus having a high etching rate, such as an ICP (inductively coupled plasma) apparatus and a magnetron RIE (reactive ion etching) apparatus. The reason is as follows. The etching using such an apparatus allows time for forming the trench 15 to be shortened greatly.

[0030] As shown in FIG. 4, N- and P-type impurities are continuously ion-implanted at a low angle into the inner wall of the trench 15 through the opening 14, thereby forming N- and P-type impurity regions 16 and 17. The N- and P-type impurities are ion-implanted into both inner walls of the trench 15 at once; however, they can be done into one of the inner walls first and then into the other inner wall. A wafer-spin type ion implanter can be used for ion implantation into both the inner walls of the trench 15.

[0031] The N- and P-type impurities are selected such that the diffusion constant of the P-type impurities becomes larger than that of the N-type impurities. In the N-channel DTMOS, arsenic (As) is used as N-type impurities and boron (B) is used as P-type impurities. In this case, arsenic is ion-implanted under conditions that an acceleration voltage is 40 keV and a dose is 2.5 ×

10^{13} cm^{-2} and so is boron under the same conditions.

[0032] In order to perform the ion implantation into the trench 15 deeply, the impurities need to be ion-implanted at such an angle that they can reach the sides of the substrate 11 on the bottom portion of the trench 15 or the opening of the mask layer 13 needs to be sufficiently broadened. When the depth of the trench 15 is 60 μm, the thickness of the semiconductor layer 12 is 56 μm, and the angle of ion implantation to the vertical direction is 7°, the mask layer 13 requires an about-7-μm-width opening.

[0033] As illustrated in FIG. 5, a thermal oxide film 18 having a thickness of about 500Å is formed on the surface of the trench 15 by thermal oxidation.

[0034] As illustrated in FIG. 6, the N- and P-type impurities are diffused at once by thermal oxidation under conditions that temperature is 1150°C and diffusion time is 270 minutes, with the result that a first N-type pillar layer 19 and a P-type pillar layer 20 forming a super junction structure are formed. The pillar layers, however, can be formed in different steps. For example, after N-type impurities are ion-implanted and thermally diffused, P-type impurities can be ion-implanted and thermally diffused, and vice versa. The process, however, can be executed more easily when two different impurities are implanted in sequence to form the N- and P-type impurity regions 16 and 17 than when two different impurities are implanted separately from each other.

[0035] If arsenic is used as the N-type impurities and boron is used as the P-type impurities, the diffusion constant of arsenic at 1150°C is about 1.8×10^{-2} μm^2/h and that of boron is about 1.1×10^{-1} μm^2/h. In other words, the diffusion constant of boron is an order of magnitude greater than that of arsenic. Thus, arsenic is diffused by about 2.5 μm to 3.0 μm and boron is diffused by about 7.5 μm in the lateral direction (which is perpendicular to the depth direction of the trench) from the inner walls of the trench 15.

[0036] As shown in FIG. 7, the mask layer 13 and thermal oxide film 18 are removed using, e.g., a fluorine-type chemical solution.

[0037] As shown in FIG. 8, an oxide film 21 having a thickness of about 1.2 μm is formed on the surfaces of the semiconductor layer 12 and trench 15. Then, a buried layer 22 is formed on the oxide film 21, with the result that the trench 15 is filled with the buried layer 22 and oxide film 21.

[0038] Referring to FIG. 9, the buried layer 22 and oxide film 21 are removed by CMP (chemical mechanical polishing) or etching so as to expose the surface of the semiconductor layer 12. The surfaces of these layers 12 and 22 are therefore flattened.

[0039] As illustrated in FIG. 10, a mask layer 23 composed of, e.g., a thermal oxide film having a thickness of 4000Å is formed on the flattened surfaces of the layers 12 and 22. Then, the mask layer 23 is patterned by lithography and etching to form an opening 24 through which part of the surface of the semiconductor layer 12

is exposed. The opening 24 is formed so as to expose the surface of the semiconductor layer 12 in the vicinity of the upper end portion of the trench 15. The width of the opening 24 is, for example, 0.2 μm to 3.0 μm. The reason is as follows. If the width is smaller than 0.2 μm, ion implantation for forming a second N-type pillar layer 25 (described later) cannot be performed sufficiently. If the width is larger than 3.0 μm, a region for a base layer 26 (described later) cannot be secured or the channel length is shortened. The width of the opening 24 is indicated by a numeric value corresponding to the respective dimensions exemplified in the first embodiment and can be varied appropriately with variations in the dimensions.

[0040]   For example, phosphorus (P) is ion-implanted through the opening 24 as N-type impurities and then thermally diffused. The ion implantation of phosphorus is performed under conditions that an acceleration voltage is 40 keV and a dose is 2.0×10^{12} cm^{-2}. The diffusion is performed in an atmosphere of nitrogen under conditions that temperature is 1150°C and diffusion time is 70 minutes, with the result that a second N-type pillar layer 25 is formed on either side of the trench 15 in the upper area of the semiconductor layer 12. The layer 25 contacts the first N-type pillar layer 19. After that, the mask layer 23 is removed.

[0041]   A base layer 26 is selectively formed in a surface area of the semiconductor layer 12 and a source layer 27 is selectively formed in the surface area of the base layer 26 using a known technique, as shown in FIG. 1. A gate electrode 28 is formed on the semiconductor layer 12 with a gate insulation film interposed therebetween and covered with an interlayer insulation film 29. A source electrode 30 is formed on the interlayer insulation film 29 and a drain electrode 31 is formed on the undersurface of the substrate 11. The base layer 26 and source layer 27 can be formed in self-alignment using the gate electrode 28 as a mask

[0042]   FIG. 11 is a cross-sectional view of part of the semiconductor device shown in FIG. 1, which shows a contour map of the distribution of concentrations of the N-type pillar layer. FIG. 12 shows the distribution of concentrations in the cross-sectional view taken along line XII-XII of FIG. 11. FIG. 13 shows the distribution of concentrations in the cross-sectional view taken along line XIII-XIII of FIG. 11. The following are descriptions of the distribution of concentrations of the semiconductor device according to the first embodiment.

[0043]   Referring to FIG. 11, since the second N-type pillar layer 25 is formed, a region whose impurity concentration is equal to or higher than that of the first N-type pillar layer 19 is formed up to the surface of the semiconductor layer 12.

[0044]   As depicted in FIG. 12, the concentration Nd of arsenic in the semiconductor layer 12 increases toward the sides of the trench 15. In other words, the N-type pillar layer 19 is formed on either side of the trench 15. On the other hand, the concentration Nd of arsenic

in the central area of the semiconductor layer 12 between trenches 15 is low and the concentration Nd of boron is higher than that of arsenic. The P-type pillar layer 20 is formed in this area. The impurity concentration Nd of the first N-type pillar layers 19 formed on the sides of the pillar 15 is about 5×10^{15} cm^{-3}. The concentration Nd of phosphorus is almost constant at about 2×10^{14} cm^{-3}.

[0045]   As shown in FIG. 13, the concentration of arsenic for forming the first N-type pillar layer 19 decreases toward the surface of the semiconductor layer 12, while that of phosphorus for forming the second N-type pillar layer 25 increases. As a result of combination of these impurity concentrations, the impurity concentration Nd of the N-type pillar layer 25 formed in the surface area of the semiconductor layer 12 becomes about 1×10^{16} cm^{-3}. In other words, the impurity concentration Nd of the second N-type pillar layer 25 is about ten times as high as that of the first N-type pillar layer 19. The former impurity concentration can be more than ten times as high as the latter impurity concentration. Further, the impurity concentration Nd of a boundary between the first and second N-type pillar layers 19 and 25 is lower than that of the first N-type pillar layer 19. The concentration Nd of boron for forming the P-type pillar layer 20 is almost constant in the depth direction of the semiconductor layer 12.

[0046]   According to the first embodiment, the second N-type pillar layer 25 is formed on either side of the trench 15 in the upper area of the semiconductor layer 12 and contacts the first N-type pillar layer 19. Therefore, even though ions cannot be implanted sufficiently into the inner wall of the trench 15 in the upper area of the semiconductor layer 12 due to a projection of the mask layer 13, an N-type diffusion region can be formed up to the top surface of the semiconductor layer 12 if the second N-type pillar layer 25 is formed later on. Consequently, a current path can be secured between the source and drain.

[0047]   The second N-type pillar layer 25 whose concentration is higher than that of the first N-type pillar layer 19 is formed on either side of the trench 15 in the upper area of the semiconductor layer 12. It is thus possible to ease the concentration of current on either side of the trench 15 in the upper area of the semiconductor layer 12. Accordingly, the resistance of elements can be decreased.

[0048]   It has been described above that the base layer 26 contacts the first and second N-type pillar layers 19 and 25. The advantage of the first embodiment described above also can be obtained while the base layer 26 does not contact the first and second N-type pillar layers 19 and 25. Any additional advantage obtained when the base layer 26 does not contact the layers 19 and 25 will be described below.

[0049]   For a first modification, a PN junction can be formed only between the base layer 26 and the second N-type pillar layer 25 as shown in FIG. 14A, with the

result that the P-type pillar layer 20 having lower concentration than the base layer 26 exists between the base layer 26 and the first N-type pillar layer 19. An electric field can thus be prevented from concentrating on the corner portion of the base layer 26 when a reverse bias is applied between the drain and source. It is thus possible to prevent the semiconductor device from decreasing in withstand voltage.

[0050] For a second modification, as shown in FIG. 14B, the P-type pillar layer 20 can be left to the surface of the semiconductor layer 12 if the second N-type pillar layer 25 or base layer 26 is decreased in length in the lateral direction. In other words, the base layer 26 and second N-type pillar layer 25 do not contact each other. Since, in this case, an inverted region is formed in the P-type pillar layer 20, no current path is cut off. Thus, the area of opposing portions of the drain (second N-type pillar layer 25) and the gate electrode 28 decreases, and the drain-to-gate capacitance can be reduced while same advantage as that of the first modification can be obtained the same time. The semiconductor device can thus be operated at high speed.

[Second Embodiment]

[0051] FIG. 15 is a schematic cross-sectional view showing a semiconductor device according to a second embodiment of the present invention as a DTMOS having a vertical NPN structure.

[0052] Referring to FIG. 15, a second N-type pillar layer 35 is provided so as to extend in the lateral direction along the surface of a semiconductor layer 12. One side of the layer 35 contacts a trench 15 and the other side contacts the base layer 26, and the bottom portion thereof overlaps the top portion of a first N-type pillar layer 19. The first and second N-type pillar layers 19 and 35 serve as a source-to-drain current path.

[0053] FIG. 16 is a schematic cross-sectional view showing a manufacturing step of the semiconductor device according to the second embodiment of the present invention. A method of manufacturing the semiconductor device will now be described.

[0054] As in the first embodiment shown in FIGS. 2 to 9, a first N-type pillar layer 19 and a P-type pillar layer 20 are formed on either side of a trench 15. After that, the trench 15 is filled with a buried layer 22 and the surfaces of a semiconductor layer 12 and the buried layer 22 are flattened.

[0055] As illustrated in FIG. 16, the mask layer 23 shown in FIG. 9 is not formed, but N-type impurities such as phosphorus are ion-implanted into the whole of the flattened surfaces of the layers 12 and 22 and then thermally diffused. As a result, a second N-type pillar 35 is formed on the surface of the semiconductor layer 12 in contact with the first N-type pillar layer 19. When phosphorus is used as N-type impurities, the ion implantation is performed under conditions that an acceleration voltage is 40 keV and a dose is 1.5×10^{12} cm^{-2} and the

diffusion is done in an atmosphere of nitrogen under conditions that temperature is 1150°C and diffusion time is 20 minutes.

[0056] The second N-type pillar layer 35 is formed on the entire surface of the semiconductor layer 12. This formation presents no problem if the concentration of the second N-type pillar layer 35 is considerably lower than that of a P-type base layer 26 (described later) formed in the layer 35.

[0057] Then, a high-concentration P+-type base layer 26 is selectively formed in the surface area of the semiconductor layer 12 using a known technique as shown in FIG. 15. When boron is used as P-type impurities, the ion implantation is performed under conditions that an acceleration voltage is 60 keV and a dose is 3.0×10^{14} cm^{-2}. The diffusion is done in an atmosphere of nitrogen under conditions that temperature is 1150°C and diffusion time is 230 minutes. After that, a high-concentration source layer 27 is selectively formed in the surface area of the base layer 26, as in the first embodiment. Then, a gate electrode 28 is formed on the semiconductor layer 12 with a gate insulation film interposed therebetween, and an interlayer insulation film 29, a source electrode 30, and a drain electrode 31 are formed.

[0058] FIG. 17 is a cross-sectional view of the semiconductor device according to the second embodiment of the present invention, which shows a contour map of the distribution of concentrations of the N-type pillar layer. FIG. 18 shows the distribution of concentrations in the cross-sectional view taken along line XVIII-XVIII of FIG. 17. FIG. 19 shows the distribution of concentrations in the cross-sectional view taken along line XIX-XIX of FIG. 17. The following are descriptions of the distribution of concentrations of the semiconductor device according to the second embodiment.

[0059] Since the second N-type pillar layer 35 is formed, a region whose impurity concentration is equal to or higher than that of the first N-type pillar layer 19 is formed up to the surface of the semiconductor layer 12 as shown in FIG. 17. The impurity concentration of the N-type pillar layer 35 is uniform in the lateral direction (which is perpendicular to the depth direction of the trench 15) of the surface of the semiconductor layer 12.

[0060] In the case of FIG. 17, when an amount of projection of the mask layer 13 is about 0.4 μm, ion implantation is performed into a region that is 3 μm or more deep from the surface of the semiconductor layer 12 and consequently the first N-type pillar layer 19 is formed from the depth of 1 μm from the surface of the semiconductor layer 12.

[0061] As shown in FIG. 18, the concentration Nd of arsenic in the semiconductor layer 12 increases toward the sides of the trench 15. The N-type pillar layer 19 is therefore formed on either side of the trench 15. On the other hand, the concentration Nd of arsenic in the central area of the semiconductor layer 12 between trenches 15 is low and the concentration Nd of boron is higher than that of arsenic. The P-type pillar layer 20 is there-

fore formed. The impurity concentration Nd of the first N-type pillar layer 19 formed on either side of the pillar 15 is about 5×10^{15} cm^{-3}. The concentration Nd of phosphorus, which is implanted when the semiconductor layer 12 is formed, is almost constant at 2×10^{14} cm^{-3}. The distribution of concentrations in the cross-sectional view taken along line XVIII-XVIII of FIG. 17 is the same as that in the first embodiment shown in FIG. 12.

[0062] As depicted in FIG. 19, the concentration of arsenic for forming the first N-type pillar layer 19 decreases toward the surface of the semiconductor layer 12, while that of phosphorus for forming the second N-type pillar layer 35 increases abruptly. As a result of combination of these impurity concentrations, the impurity concentration Nd of the N-type pillar layer 35 formed in the surface area of the semiconductor layer 12 is about 1×10^{16} cm^{-3}. In other words, the impurity concentration Nd of the second N-type pillar layer 35 is about ten times as high as that of the first N-type pillar layer 19. The former impurity concentration can be more than ten times as high as the latter impurity concentration. The concentration Nd of boron for forming the P-type pillar layer 20 is almost constant in the depth direction of the semiconductor layer 12.

[0063] The same advantage as that of the first embodiment can be obtained from the second embodiment.

[0064] Since a step of forming the mask layer 23 and a step of patterning it are unnecessary, the process of the second embodiment is simpler than that of the first embodiment.

[0065] According to the second embodiment, the impurity concentration of the N-type pillar layer 35 can be uniformed in the lateral direction of the surface of the semiconductor layer 12. Thus, the concentration of current on either side of the trench 15 in the upper area of the semiconductor layer 12 can be eased more greatly than that in the first embodiment. Accordingly, the resistance of the devices can be decreased further.

[0066] It is needless to say that the same advantage as that of the first embodiment can be obtained if the base layer 26 does not contact the first and second N-type pillar layers 19 and 35.

[Third Embodiment]

[0067] FIG. 20 is a schematic cross-sectional view showing a semiconductor device according to a third embodiment of the present invention as a DTMOS having a vertical NPN structure. Referring to FIG. 20, a gate electrode 28 is not formed above a trench 15 but separates from one end of the trench 15 and extends onto a channel region between one end of a base layer 26 and that of a source layer 27. The other structure is the same as that of the first embodiment.

[0068] FIG. 21 is a schematic cross-sectional view

showing a manufacturing step of the semiconductor device with the above-described structure. As in the first embodiment shown in FIGS. 2 to 9, a trench 15, a first N-type pillar layer 19, a P-type pillar layer 20, and a buried layer 22 are formed.

[0069] As illustrated in FIG. 21, a gate insulation film 51 is formed and then a conductive film is formed on the gate insulation film 51. The conductive film is patterned by lithography and etching, thus forming a gate electrode 28 that separates from one end of the trench 15 and extends onto a channel region between one end of the base layer 26 and that of the source layer 27. Then, a mask layer 52 is formed on the semiconductor layer 12. The mask layer 52 has substantially the same end portion as that of the gate electrode 28. After that, ion implantation is performed using the gate electrode 28 as a mask to form a second N-type pillar layer 25 in self-alignment. Proper alignment is not therefore required when the mask layer 52 is patterned.

[0070] As depicted in FIG. 20, the mask layer 52 is removed and then ion implantation is performed using the gate electrode 28 as a mask to form a base layer 26 in self-alignment. The second N-type pillar layer 25 and base layer 26 can be formed using the mask layer 52 as a mask. After that, a source layer 27, an interlayer insulation film 29, a source electrode 30, and a drain electrode 31 are formed through the same steps as those of the first embodiment. A wiring layer comprising conductive layer of polysilicon or the like can be formed on the gate electrodes 28, with the result that wiring resistance of the gate electrodes 28 can decrease.

[0071] The same advantages as those of the first and second embodiments can be obtained from the third embodiment.

[0072] According to the third embodiment, the second N-type pillar layer 25 is formed in self-alignment using the gate electrode 28 as a mask. Consequently, the second N-type pillar layer 25 can be formed without causing any misalignment between the layer 25 and electrode 28. As mentioned above, the base layer 26 is also formed in self-alignment using the gate electrode 28 as a mask. Therefore, misalignment between the second pillar layer 25 and the base layer 26 can be avoided.

[0073] The area of opposing portions of the drain (second N-type pillar layer 25) and the gate electrode 28 can be made much smaller than that in the first and second embodiments. Accordingly, the drain-to-gate capacitance can be reduced further and the semiconductor device can be operated at high speed. Furthermore, the wiring layer provided on the gate electrode 28 can decrease a wiring resistance of the gate electrode 28, while the drain-to-gate capacitance can be reduced.

[0074] When the first N-type pillar layer 19 is formed by ion implantation through the inner walls of the trench 15, the impurity concentration of the layer 19 increases toward the sides of the trench 15. For this reason, when a reverse bias is applied between the drain and source, the depletion of the high-concentration portion is de-

layed. According to the third embodiment, since the area of opposing portions between the high-concentration portion and the gate electrode 28 can be decreased, the capacitance can be reduced; consequently, the semiconductor device can be operated at high speed.

Claims

1. A semiconductor device comprising:

   a semiconductor substrate (11) of a first conductivity type;
   a semiconductor layer (12) provided on the semiconductor substrate (11);
   a trench (15) extending in a depth direction toward the semiconductor substrate (11) from a surface of the semiconductor layer (12);
   a first region (19) of the first conductivity type formed in the depth direction on and along a side of the trench (15) in the semiconductor layer (12), a bottom of the first region (19) contacting the semiconductor substrate (11);
   a second region (25) of the first conductivity type formed in a surface area of the semiconductor layer (12) and close to the side of the trench (15), the second region (25) contacting the first region (19);
   a third region (26) of the second conductivity type formed in the surface area of the semiconductor layer (12);
   a fourth region (27) of the first conductivity type formed in a surface area of the third region (26); and
   a gate electrode (29) provided on a surface of the third region (26) between the second region (25) and the fourth region (27), a gate insulation film being interposed between the gate electrode (29) and the second region (25).

2. The semiconductor device according to claim 1, the first and second regions (19, 25) contact the third region (26) respectively.

3. The semiconductor device according to claim 1, **characterized in that** the first region (19) separates from an end of the third region (26) and the second region (25) contacts the third region (26).

4. The semiconductor device according to claim 1, **characterized in that** the first and second regions (19, 25) separate from an end of the third region (26).

5. The semiconductor device according to claim 1, **characterized in that** the gate electrode (29) extends onto the trench (15).

6. The semiconductor device according to claim 1, **characterized in that** the second region (25) is formed in self-alignment with the gate electrode (29).

7. The semiconductor device according to claim 1, **characterized in that** impurity concentration of a surface of the second region (25) is equal to or higher than that of a portion of the first region (19) which is formed on the side of the trench (15) and close to the trench (15).

8. The semiconductor device according to claim 1, **characterized in that** impurity concentration of a surface of the second region (25) is almost uniform in a lateral direction.

9. The semiconductor device according to claim 1, **characterized in that** impurity concentration of the second region (25) is more than ten times as high as that of the first region (19).

10. The semiconductor device according to claim 1, **characterized in that** impurity concentration of a boundary between the first region (19) and the second region (25) is lower than that of the first region (19).

11. A semiconductor device comprising:

    a semiconductor substrate (11) of a first conductivity type;
    a semiconductor layer (12) of a second conductivity type provided on the semiconductor substrate (11);
    a trench (15) extending in a depth direction toward the semiconductor substrate (11) from a surface of the semiconductor layer (12), the trench (15) buried with a filling layer;
    a first region (19) of the first conductivity type formed in the depth direction on and along a side of the trench (15) in the semiconductor layer (12), a bottom of the first region (19) contacting the semiconductor substrate (11);
    a second region (25) of the first conductivity type formed in a surface area of the semiconductor layer (12) and close to the side of the trench (15), the second region (25) contacting the first region (19);
    a third region (26) of the second conductivity type formed in the surface area of the semiconductor layer (12);
    a fourth region (27) of the first conductivity type formed in a surface area of the third region (26); and
    a gate electrode (29) provided on a surface of the third region (26) between the second region (25) and the fourth region (27), a gate insulation

film being interposed between the gate electrode (29) and the second region (25).

12. The semiconductor device according to claim 11, the first and second regions (19, 25) contact the third region (26) respectively.

13. The semiconductor device according to claim 11, **characterized in that** the first region (19) separates from an end of the third region (26) and the second region (25) contacts the third region (26).

14. The semiconductor device according to claim 11, **characterized in that** the first and second regions (19, 25) separate from an end of the third region (26).

15. The semiconductor device according to claim 11, **characterized in that** the gate electrode (29) extends onto the trench (15).

16. The semiconductor device according to claim 11, **characterized in that** the second region (25) is formed in self-alignment with the gate electrode (29).

17. The semiconductor device according to claim 11, **characterized in that** the impurity concentration of the third region (26) is higher than that of the semiconductor layer (12).

18. The semiconductor device according to claim 11, **characterized in that** impurity concentration of a surface of the second region (25) is equal to or higher than that of a portion of the first region (19) which is formed on the side of the trench (15) and close to the trench (15).

19. The semiconductor device according to claim 11, **characterized in that** impurity concentration of a surface of the second region (25) is almost uniform in a lateral direction.

20. The semiconductor device according to claim 11, **characterized in that** impurity concentration of the second region (25) is more than ten times as high as that of the first region (19).

21. The semiconductor device according to claim 11, **characterized in that** impurity concentration of a boundary between the first region (19) and the second region (25) is lower than that of the first region (19).

22. A method of manufacturing a semiconductor device, comprising:

   forming a semiconductor layer (12) on a semi-

conductor substrate (11) of a first conductivity type;
forming a trench (15) having a first opening in the semiconductor layer (12), the trench (15) extending in a depth direction toward the semiconductor substrate (11);
ion-implanting first and second impurities into an inner wall of the trench (15) through the first opening;
diffusing the first impurities to form a first region (19) of the first conductivity in the depth direction on and along a side of the trench (15) in the semiconductor layer (12), a bottom of the first region (19) contacting the semiconductor substrate (11);
diffusing the second impurities to form a second region (20) of a second conductivity type in the depth direction along the first region (19) in the semiconductor layer (12), the second region (20) contacting one side of the first region (19), which is opposite to another side contacting the trench (15);
burying a filling layer (22) into the trench (15);
forming a third region (25) of the first conductivity type in a surface area of the semiconductor layer (12) and close to the side of the trench (15), the third region (25) contacting the first region (19);
forming a fourth region (26) of the second conductivity type in the surface area of the semiconductor layer (12), the fourth region (26) having impurity concentration which is higher than that of the second region (20); and
forming a fifth region (27) of the first conductivity type in a surface area of the fourth region (26).

23. The method according to claim 22, **characterized in that** the first and second impurities are selected such that a diffusion constant of the second impurities is larger than that of the first impurities.

24. The method according to claim 22, **characterized in that** the first and second impurities are ion-implanted into both inner walls of the trench (15).

25. The method according to claim 22, **characterized in that** the forming the third region (25) comprises:

   selectively forming a mask layer (23) having a second opening (24) corresponding the a position of a top of the first region (19), the mask layer being formed on the semiconductor layer (12) and the filling layer (22);
   ion-implanting third impurities into a surface of the semiconductor layer (12) through the second opening (24); and
   diffusing the third impurities.

26. The method according to claim 25, **characterized in that** the second opening (24) has a width ranging from 0.2 µm to 3.0 µm.

27. The method according to claim 22, **characterized in that** the forming the third region (25) comprises:

ion-implanting third impurities into a surface of the semiconductor layer (12); and
diffusing the third impurities.

28. The method according to claim 25, **characterized in that** the mask layer is a gate electrode (29), and the method further comprises forming a gate insulation film (51) on the semiconductor layer (12) and the filling layer (22) and then forming a gate electrode (29) on the gate insulation film (51).

5

10

15

20

25

30

35

40

45

50

55
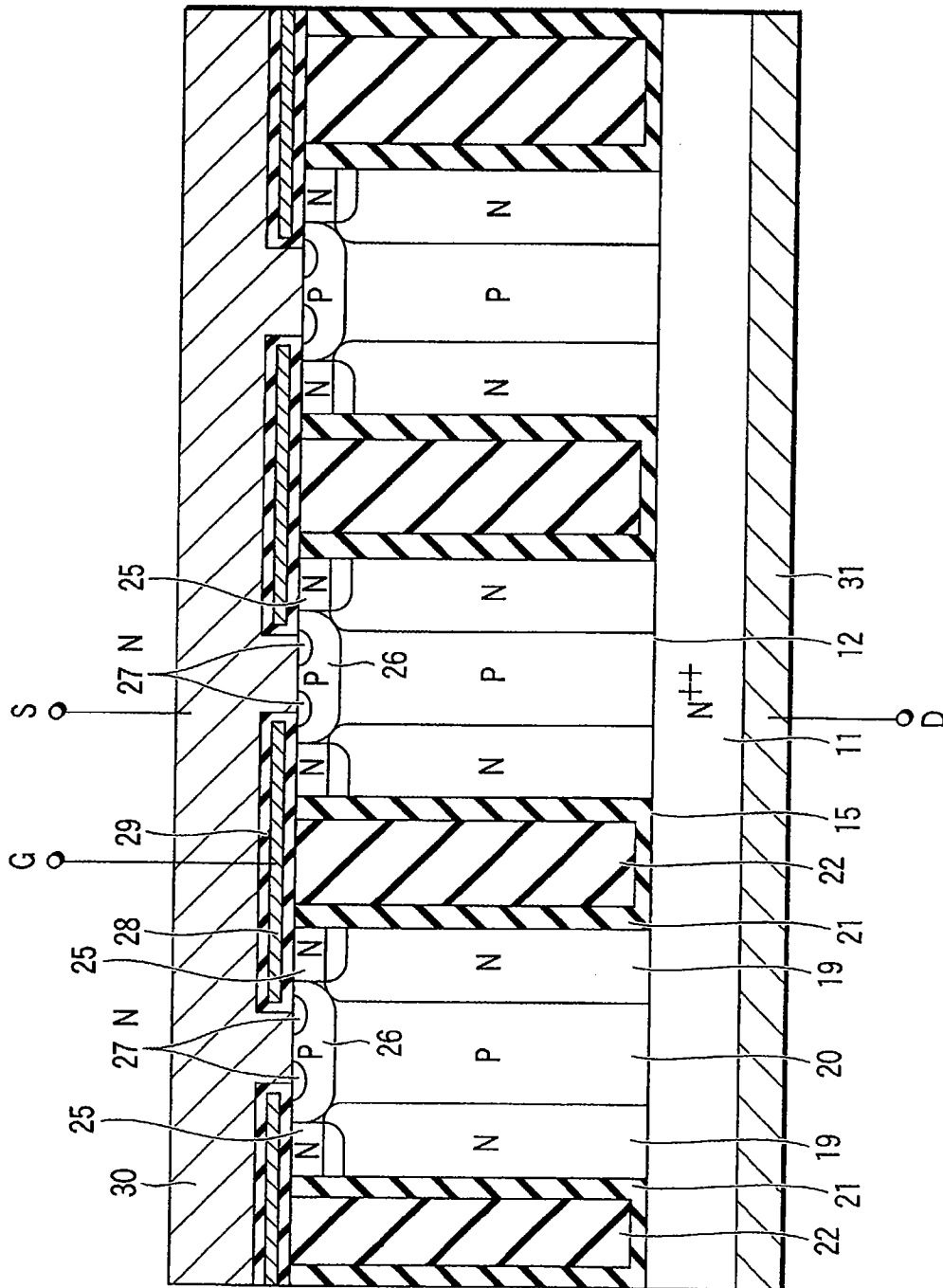
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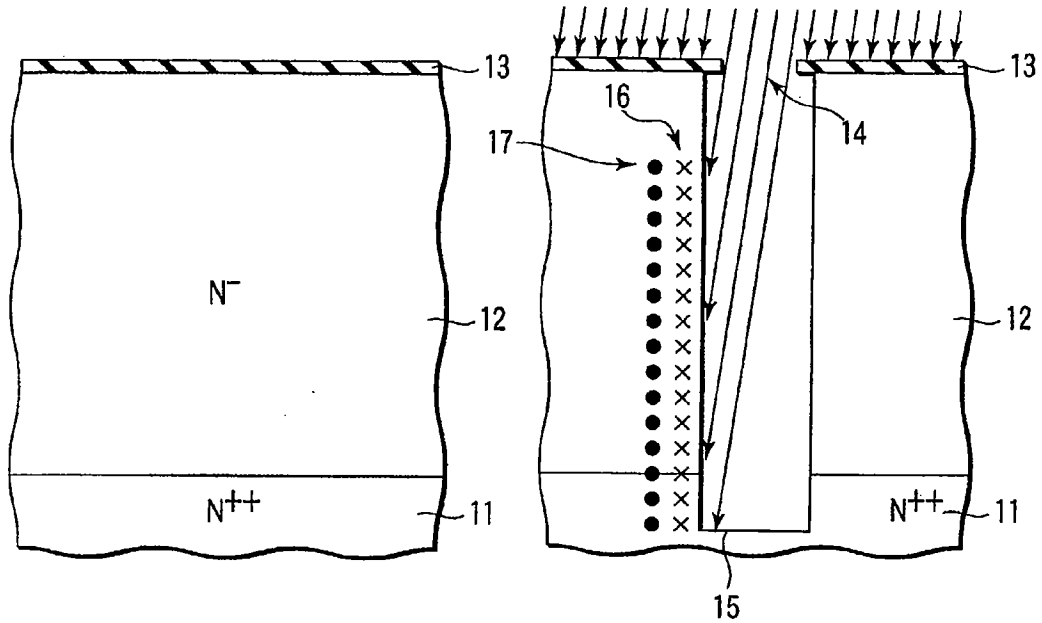
FIG.2

FIG.4
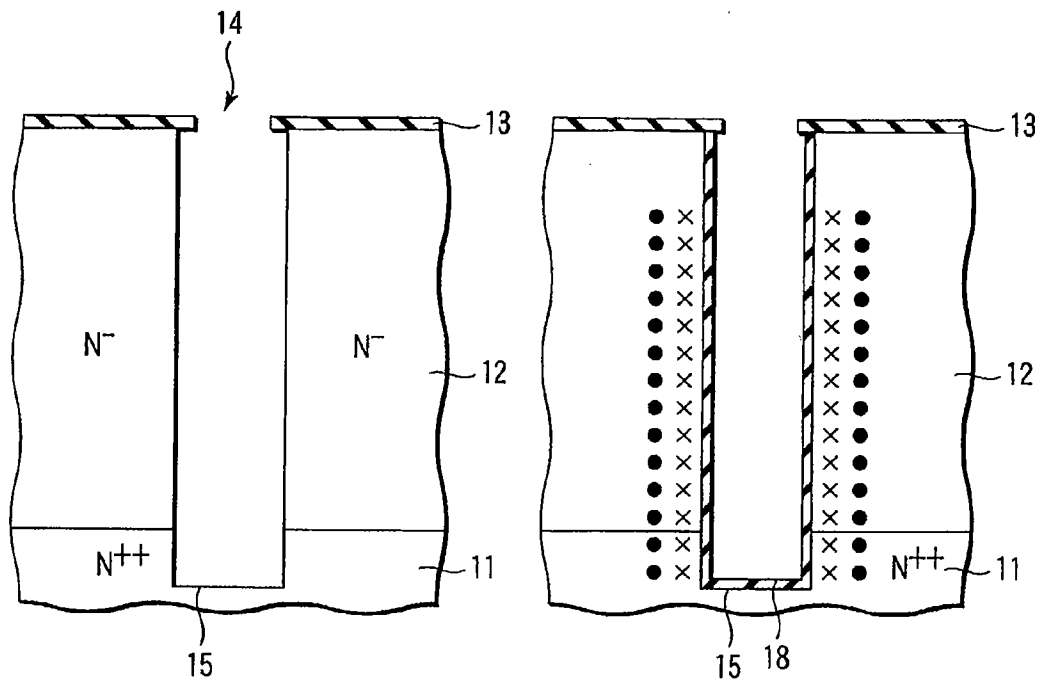
FIG.3

FIG.5
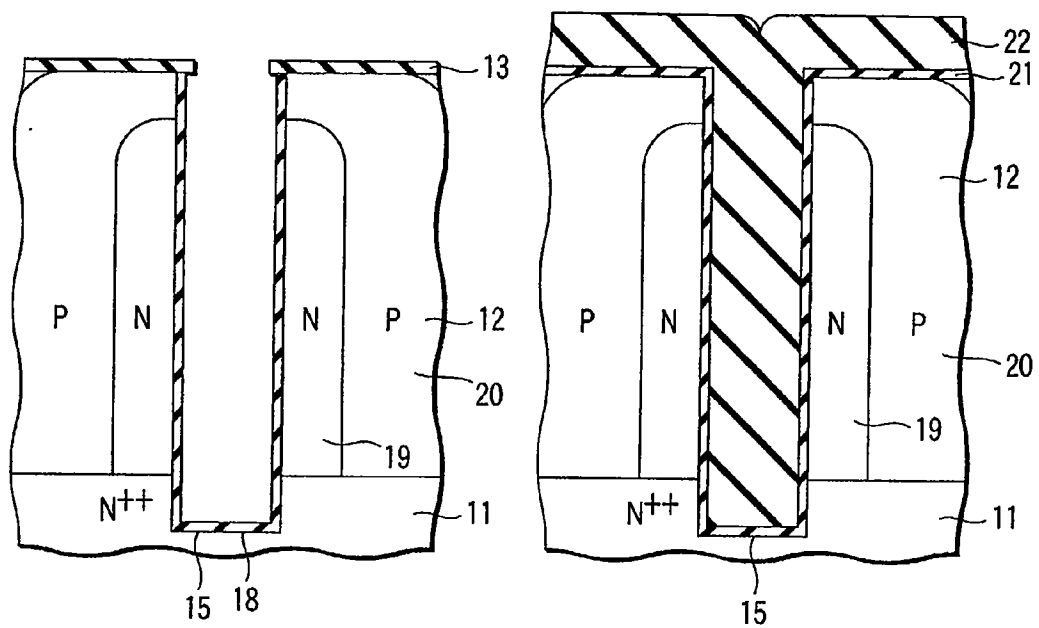
F I G. 6

F I G. 8

F I G. 7

F I G. 9

FIG. 10

FIG. 11
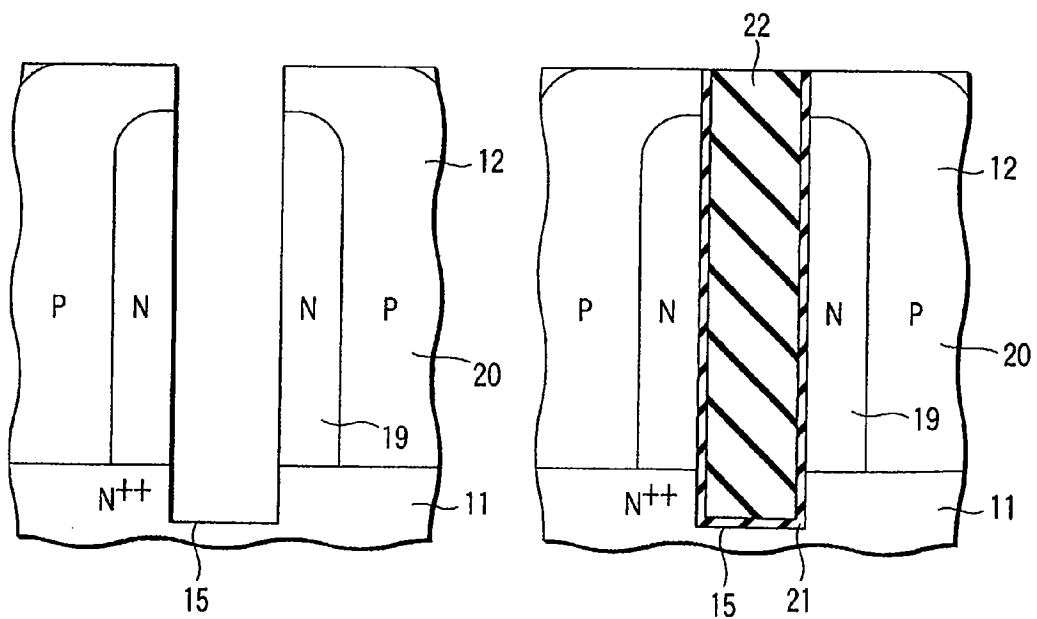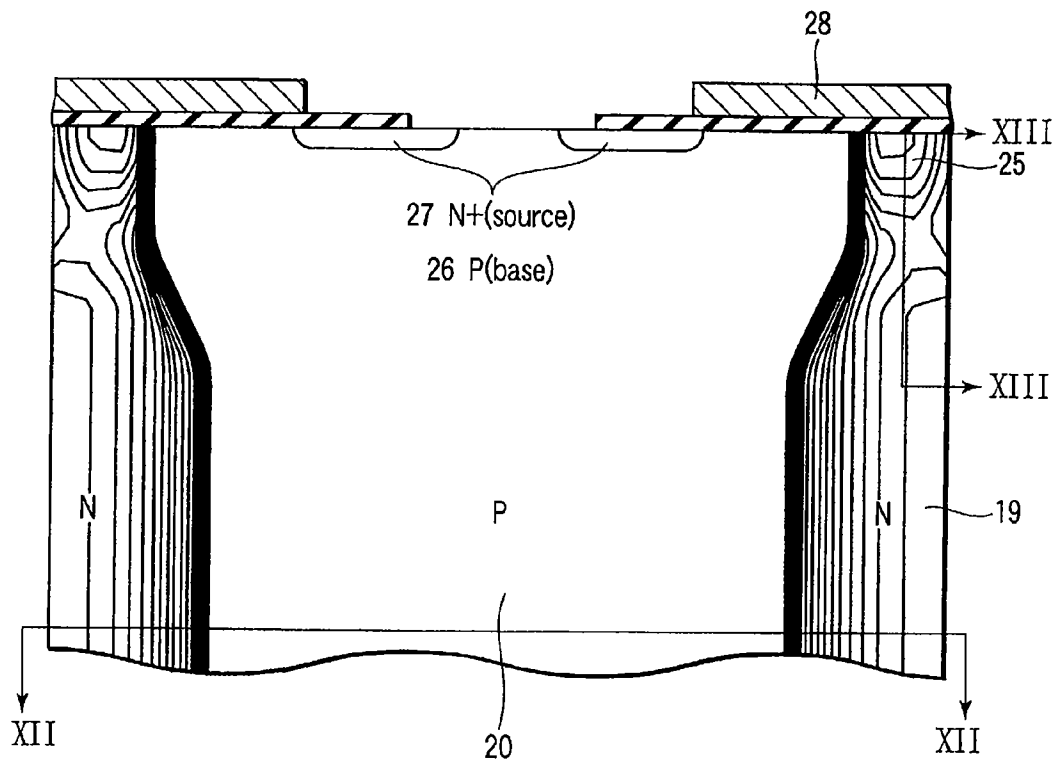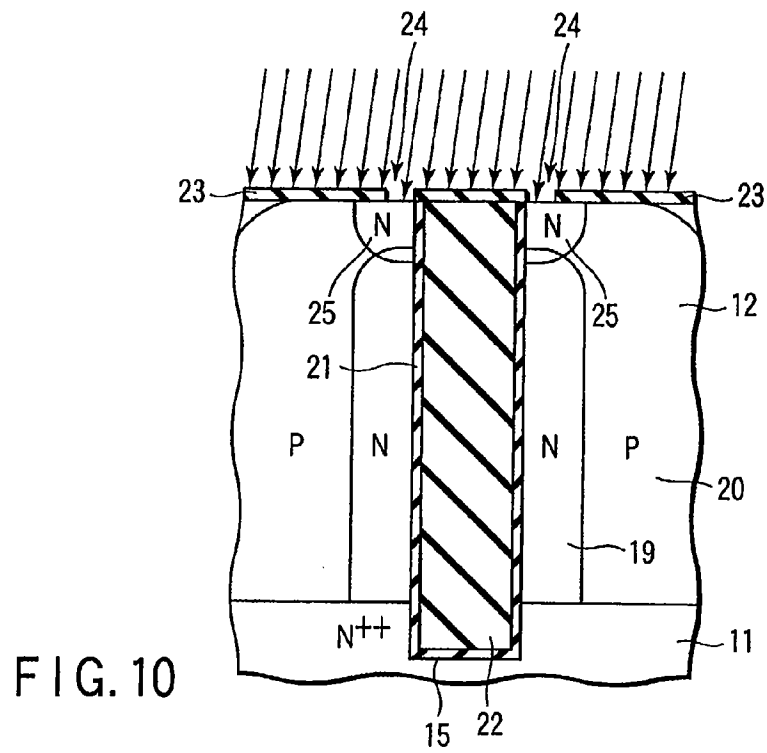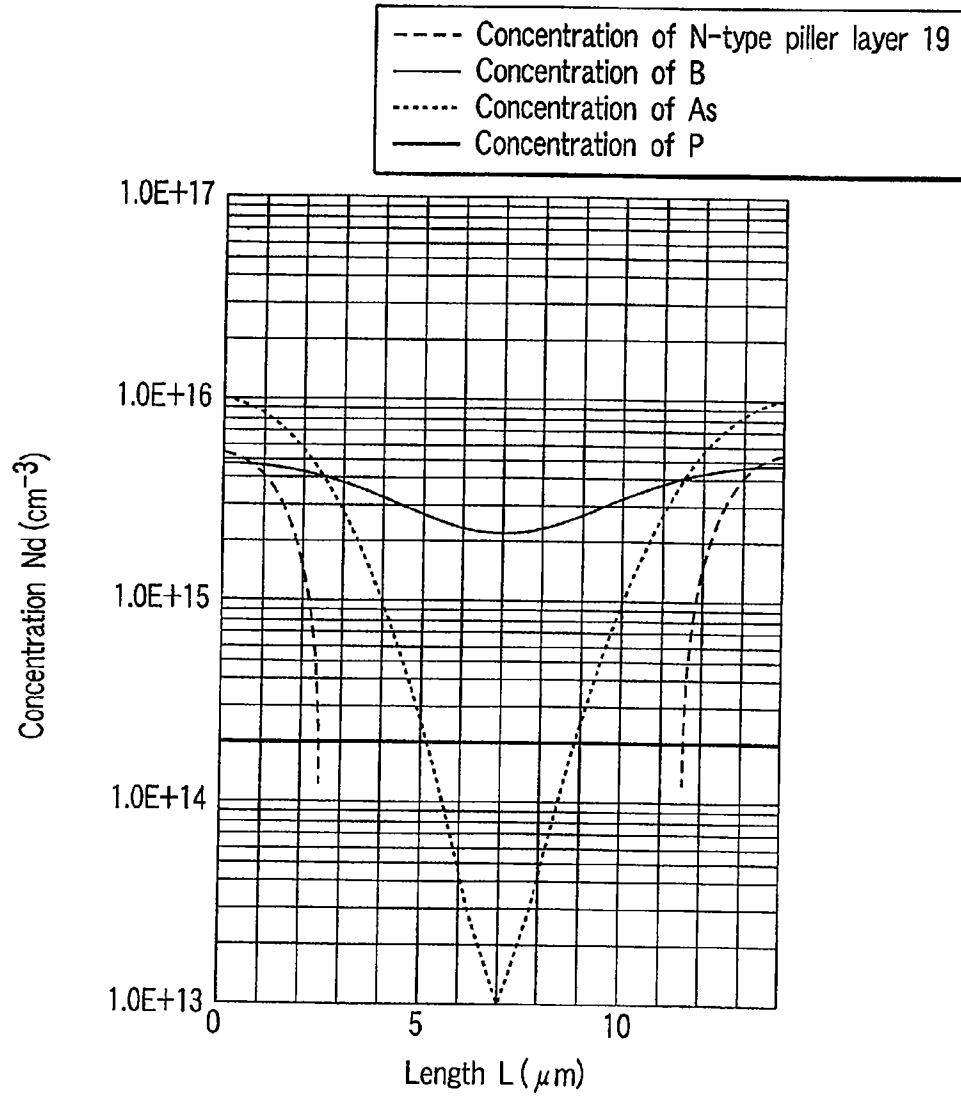
F I G. 12
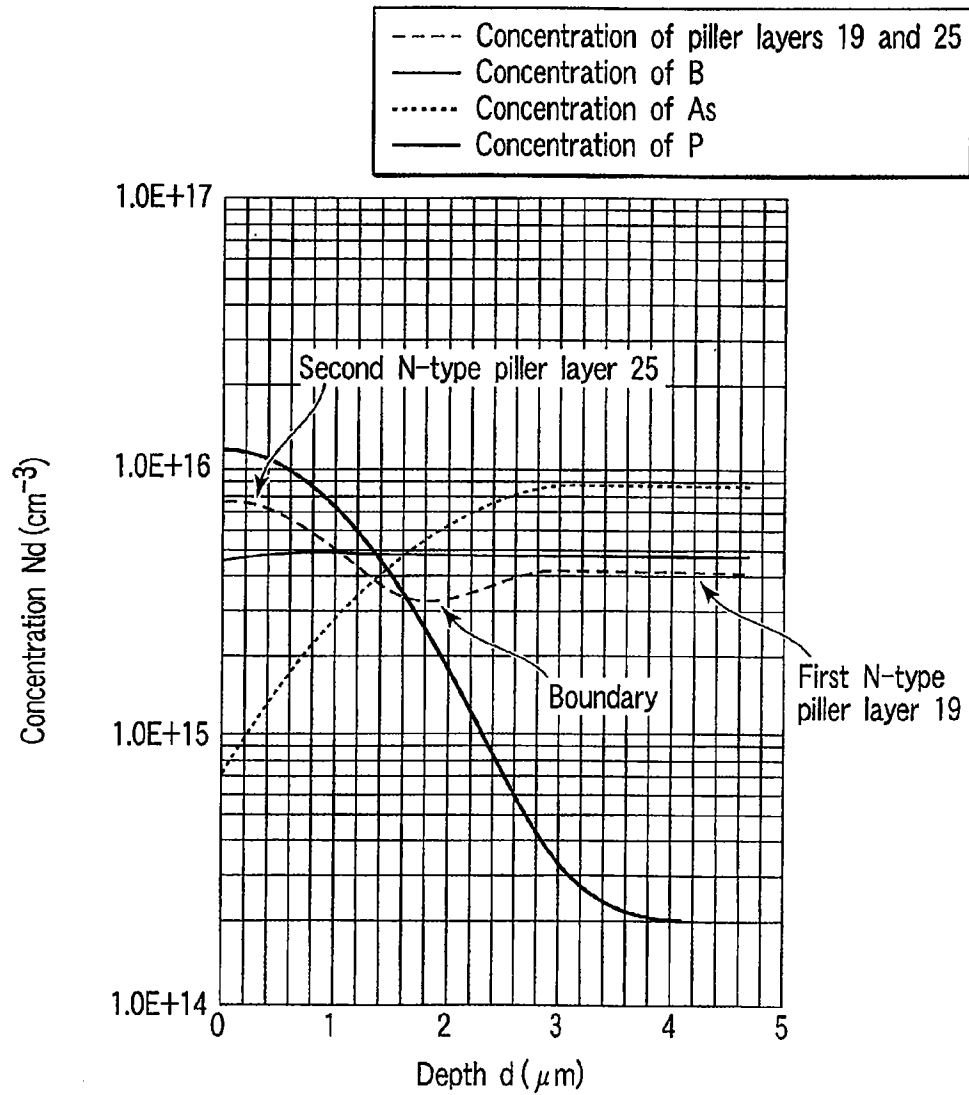
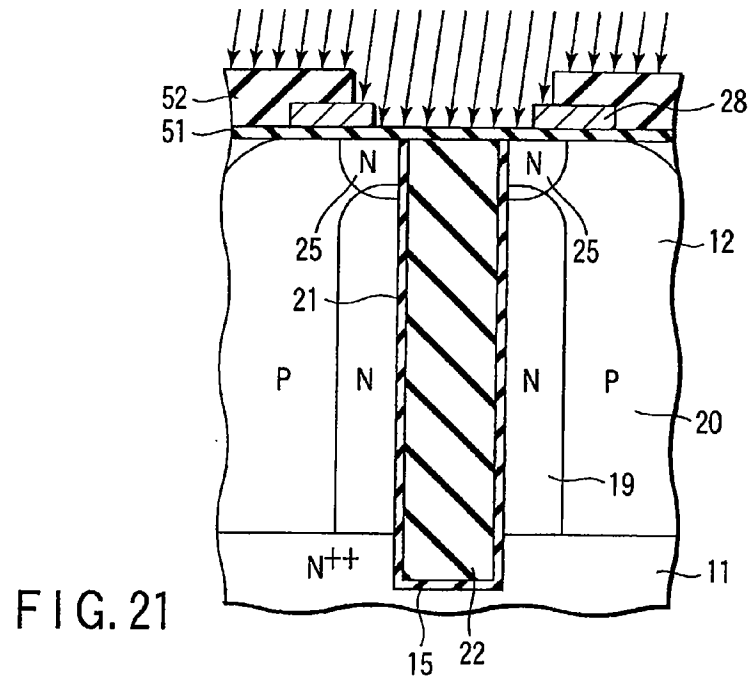F I G. 13
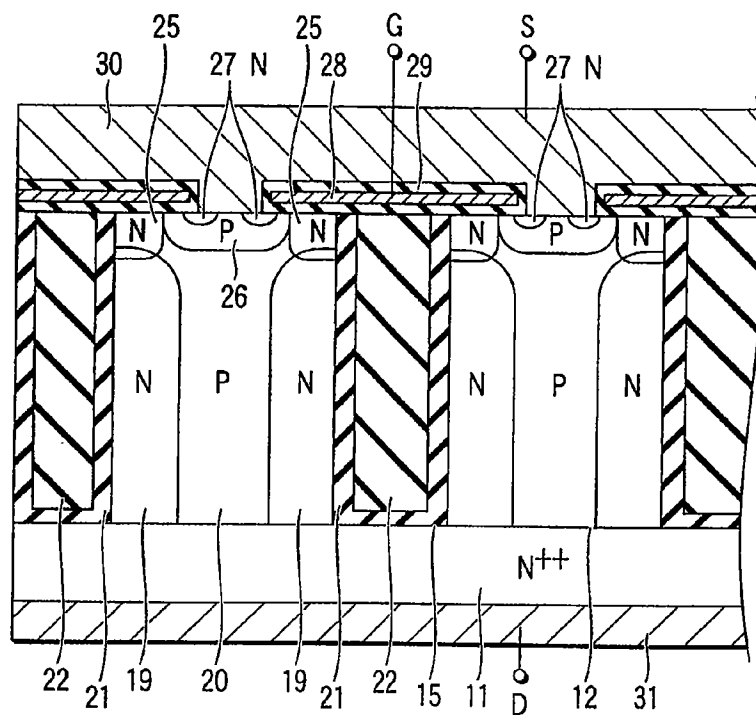
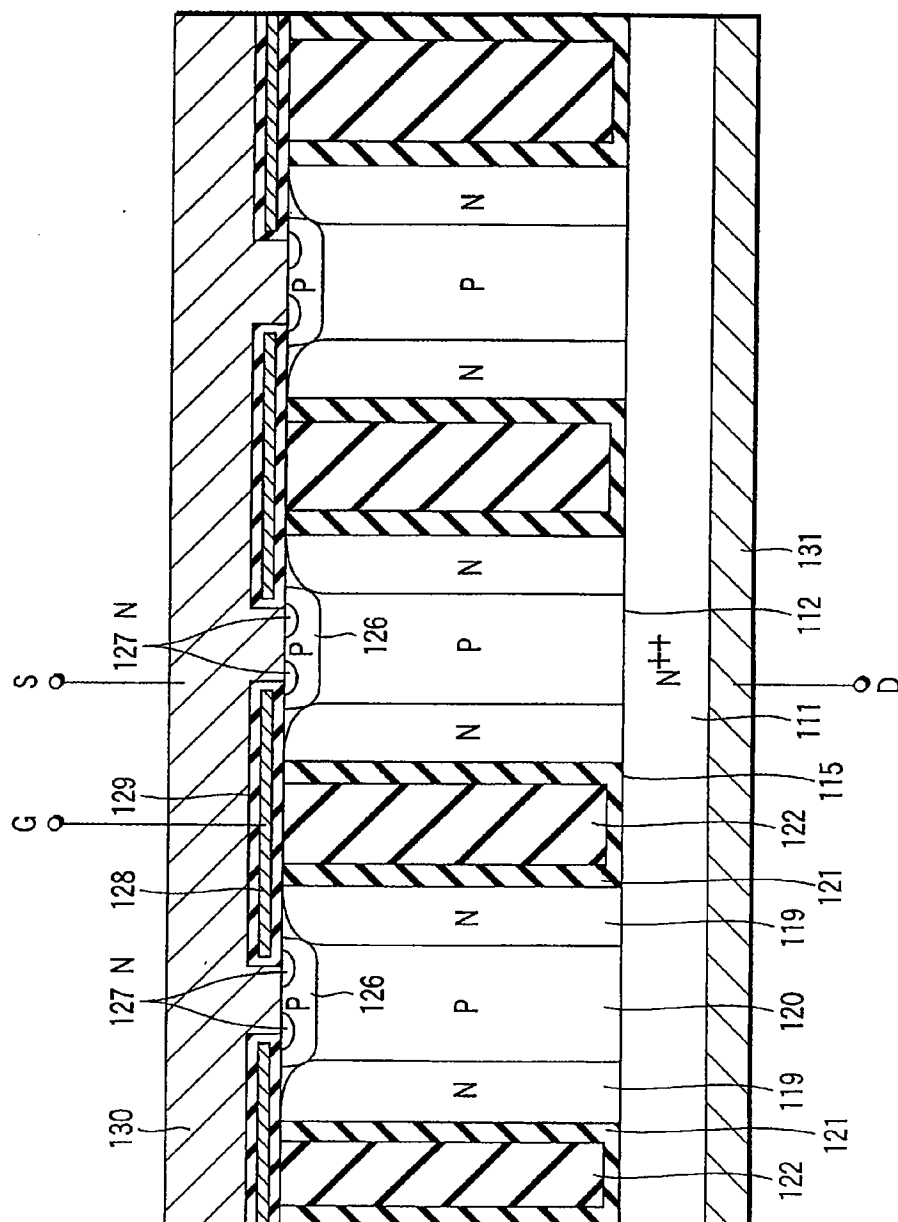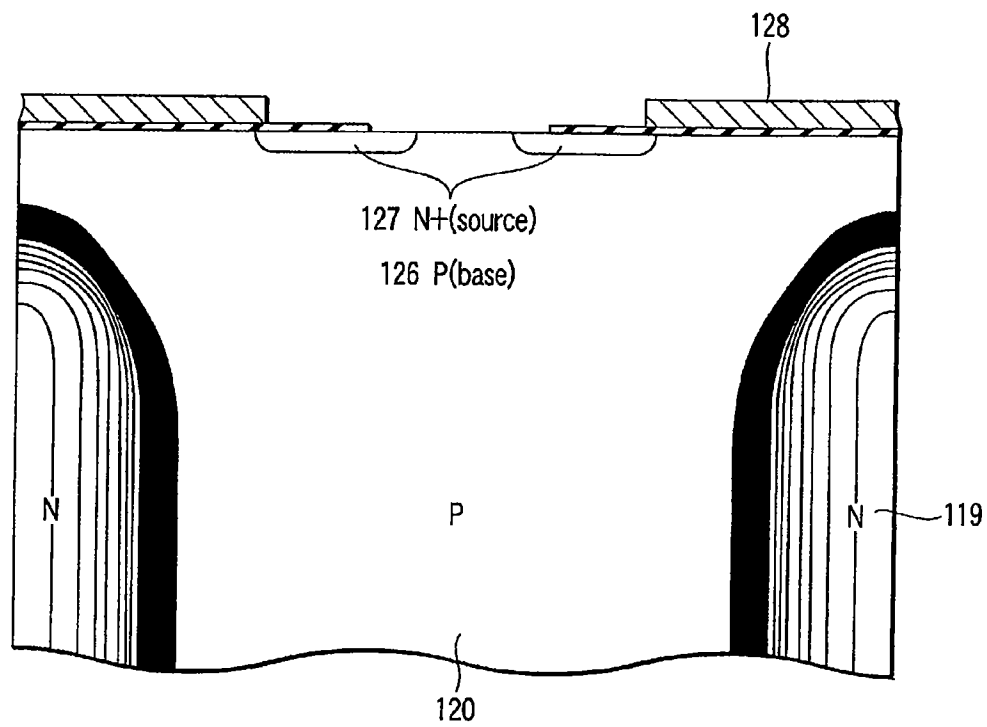FIG. 14A
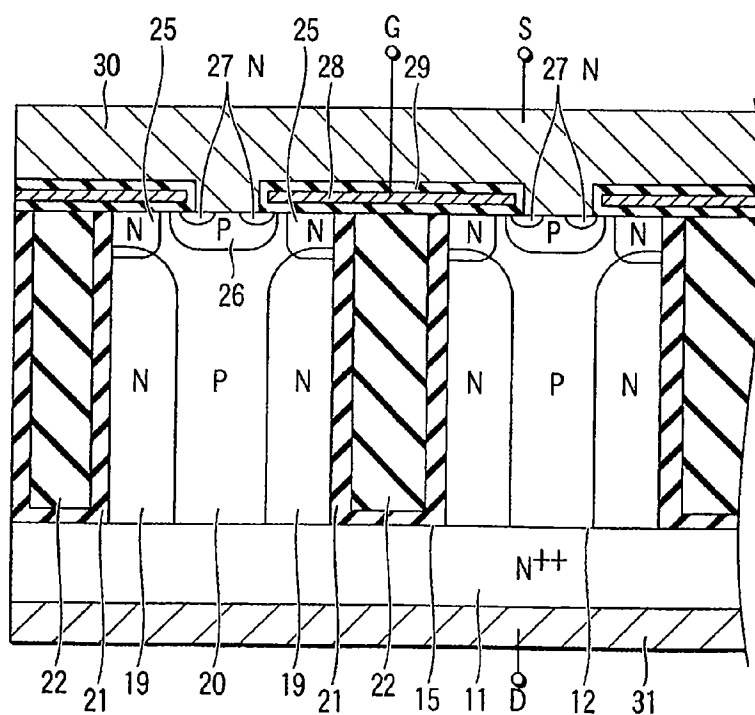
FIG. 14B

FIG. 15

FIG. 16

27 N+(source)

26 P(base)

FIG. 17

FIG. 18

F I G. 19

F I G. 20

FIG. 21

FIG. 23

FIG. 24

FIG. 22

128

127 N+(source)

126 P(base)

N

P

N ~ 119

120

F I G. 25

113

112

P   N

120   119 115

F I G. 26

122

121

112

P   N

120   119   115

F I G. 27

P   N

120   119   115 121 122

F I G. 28